IN THE CLAIMS

Please amend the Claims as follows:

1. (TWICE AMENDED) A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate;

depositing an organic dielectric layer overlying said insulating layer;

depositing an inorganic dielectric layer overlying said organic dielectric layer wherein no etch stop layer is formed between said organic dielectric layer and said inorganic dielectric layer;

etching a via pattern into said inorganic dielectric layer;

etching said via pattern into said organic dielectric layer using patterned said inorganic dielectric layer as a mask; and

thereafter etching a trench pattern into said inorganic dielectric layer wherein said organic dielectric layer acts as an etch stop to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

6. (TWICE AMENDED) A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate;

depositing an organic dielectric layer overlying said insulating layer;

depositing an inorganic dielectric layer overlying said organic dielectric layer wherein no etch stop layer is formed between said organic dielectric layer and said inorganic dielectric layer;

etching a trench pattern into said inorganic dielectric layer; and

thereafter etching a via pattern into said organic dielectric layer through said trench pattern to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

B2

11. (TWICE AMENDED) A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

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providing metal lines covered by an insulating layer overlying a semiconductor substrate;

depositing an organic dielectric layer overlying

said insulating layer;

depositing an inorganic dielectric layer overlying said organic dielectric layer wherein no etch stop layer is formed between said organic dielectric layer and said inorganic dielectric layer;

etching a via pattern into said inorganic dielectric layer; and

simultaneously etching said via pattern into said organic dielectric layer and etching a trench pattern into said inorganic dielectric layer wherein one etching recipe is used for said organic dielectric layer and a different etching recipe is used for said inorganic dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

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16. (TWICE AMENDED) A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate;

depositing an inorganic dielectric layer overlying said insulating layer;

depositing an organic dielectric layer overlying said inorganic dielectric layer wherein no etch stop

layer is formed between said inorganic dielectric layer and said organic dielectric layer;

etching a via pattern into said organic dielectric layer;

etching said via pattern into said inorganic dielectric layer using patterned said organic dielectric layer as a mask; and

thereafter etching a trench pattern into said organic dielectric layer wherein said inorganic dielectric layer acts as an etch stop to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

21. (TWICE AMENDED) A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate;

depositing an inorganic dielectric layer overlying said insulating layer;

depositing an organic dielectric layer overlying said inorganic dielectric layer wherein no etch stop layer is formed between said inorganic dielectric layer and said organic dielectric layer;

etching a trench pattern into said organic

dielectric layer; and

thereafter etching a via pattern into said inorganic dielectric layer through said trench pattern to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

26. (TWICE AMENDED) A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate;

depositing an inorganic dielectric layer overlying said insulating layer;

depositing an organic dielectric layer overlying said inorganic dielectric layer wherein no etch stop layer is formed between said inorganic dielectric layer and said organic dielectric layer;

etching a via pattern into said organic dielectric layer; and

simultaneously etching said via pattern into said inorganic dielectric layer and etching a trench pattern into said organic dielectric layer to wherein one etching recipe is used for said organic dielectric layer and a different etching recipe is used for said inorganic dielectric layer complete said forming of said

dual damascene openings in the fabrication of said integrated circuit device.